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ABBOTT, B

2823

EXAMINER

ART UNIT

PAPER NUMBER

DATE MAILED:
10/11/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

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Office Action Summary

Application No.

09/118,359

Applicant(s)

Keller et al

Examiner

Barbara Elizabeth Abbott

Group Art Unit

2823

☐ Responsive to communication(s) filed on _____

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) 1-14, 25-31, and 41-43 is/are pending in the application

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-14, 25-31, and 41-43 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 11, 13

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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In response to the office action mailed 11/12/99, applicant addresses the disposition of claim 40. Applicant is directed to page 22 of the instant application to find claim 40. This claim has been withdrawn from consideration as indicated in the office action mailed 11/12/99.

35 U.S.C. 102 Rejection

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 7, 9, 41, and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Araki et al U.S. Patent Number 5,882,994 .

Araki discloses a method of forming a floating gate comprising the steps of forming a polysilicon structure (104) over a semiconductive substrate (101), (104) having a first layer (inner portion - 140nm thick) and a second layer (outer portion- 70nm thick) atop the first layer, wherein the first layer has a higher concentration of conductivity enhancing impurity than the second layer, and wherein the inner first portion is in contact with the gate dielectric; forming a dielectric material (106) over (104); and forming a layer of conductive material (107) over (106) (Col. 3, line 13- Col. 4, line 56 and Figure 8). Applicant argues that Araki does not disclose every

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aspect of claim 1. Specifically, applicant argues that Araki discloses a three layered structure of non-doped, doped, and non-doped polysilicon to form the floating gate. The first two layers of Araki's floating gate structure can be characterized as one layer. The layer is in contact with the gate dielectric and is conductively doped. Although the applicant's argument is persuasive, claims 1 and 9 and newly added claims 41 and 42 do not overcome the rejection.

35 U.S.C. 103 Rejection

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3, 4, 5, 6, 8, 10, 11, 12, 13, 14, 25, 26, 27, 28, 29, 30, 31, 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Araki as applied to claims 1, 2, 7, and 9 above, and further in view of the following comments.

Araki discloses a dopant concentration of $1 \times 10^{20} \text{cm}^{-3}$ in the first layer and a dopant concentration of none in the second layer (Col. 5, lines 14-17). Araki does not disclose the specifically recited dopant concentration of the instant application, however, the range disclosed by Araki overlaps with the claimed range in the instant application of a concentration equal to or greater than $1 \times 10^{18} \text{cm}^{-3}$ in the first portion and less than $1 \times 10^{18} \text{cm}^{-3}$ in the second portion. (See

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MPEP 2144.05). Araki discloses that (106) is an ONO layer formed by oxidizing the substrate to form a first oxide layer over the second layer of polysilicon, forming a nitride layer over the first oxide layer, and oxidizing the substrate to form a second oxide layer over the layer of nitride.

Araki also discloses that (107), (106), and (104) are etched to form the floating gate (Col. 4, lines 44-63 and Figure 8). Araki does not disclose doping of the first polysilicon layer after forming the layer but instead deposits a doped layer. The examiner takes judicial notice that post deposition doping to form doped layers was known at the time of the applicant's invention to be a suitable method of forming doped layers. It would have been within the scope of one with ordinary skill in the art at the time of the invention to employ the known method for its known intended purpose to achieve the doped layer formation step of Araki. (See MPEP 2144.05). Araki does not

Q.25 specifically disclose that the first layer of polysilicon is doped to degree sufficient to define a sheet resistance of between 300 ohm/sq and 400 ohm/sq. The doping level disclosed by Araki overlaps with the claimed range of the instant application; therefore, because the same materials are being treated in the same manner the method of Araki would inherently result in a sheet resistance range that overlaps with the claimed range. With respect to claim 31, the step merely describes the effect of doping the first layer with a higher concentration of impurity than the second layer.

Araki discloses forming a second layer of polysilicon to have a lower dopant concentration than the first layer. Araki does not explicitly disclose that this process of doping results in a greater sheet resistance in the second layer than in the first layer. It is commonly known in the art that undoped polysilicon exhibits higher sheet-resistivity values than doped polysilicon. Araki's step

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of doping the first layer to a higher concentration than the second layer would inherently result in the second layer possessing a higher sheet resistance. Araki discloses a thickness of the first layer (inner portion) of silicon to be 140 nm and a thickness of 70 nm for the second layer (outer portion) of silicon (Col. 3, lines 30-32). Araki does not disclose the specifically recited thickness ranges of the instant application, however, the disclosed range overlaps with the claimed range in the instant application of a thickness for the inner portion to comprise at least 25%, between 25% and 75%, and less than 75% of the floating gate thickness. (See MPEP 2144.05). With respect to claims 27 and 28, Araki discloses first and second thicknesses of the first and second polysilicon layers to be 140 nm and 70 nm respectively. Araki does not disclose the specifically recited thicknesses of the instant application, however, the range disclosed by Araki overlaps with the claimed range in the instant application of a being different and that the first thickness constitutes less than or equal to 75% of the aggregate thickness of the two layers (Col. 3, lines 30-32). (See MPEP 2144.05). With respect to claim 26, Araki does not disclose that the first and second thicknesses of the polysilicon layer as being the same. However, given the substantial teaching of Araki, it would have been obvious to one with ordinary skill in the art at the time of the invention to determine the optimal thicknesses for the first and second layers through routine experimentation and optimization to achieve optimum benefits (See MPEP 2144.05). With respect to claims 29 and 30, Araki discloses a first polysilicon layer 140 nm thick and a second layer of polysilicon 70 nm thick. Araki does not disclose the specifically recited thicknesses of between 450 Angstroms and 550 Angstroms. However, given the substantial teaching of Araki, it

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would have been obvious to one with ordinary skill in the art at the time of the invention to determine the optimal thicknesses for the first and second layers through routine experimentation and optimization to achieve optimum benefits (See MPEP 2144.05). With respect to claim 14, Araki discloses a dopant concentration of $1 \times 10^{20} \text{ cm}^{-3}$ in the first layer of polysilicon (Col. 5, lines 14-17). This range overlaps with the claimed range in the instant application of greater than or equal to $1 \times 10^{18} \text{ cm}^{-3}$ for the first layer. Araki also discloses a thickness of the first layer (inner portion) of silicon to be 140 nm and a thickness of 70 nm for the second layer (outer portion) of silicon (Col. 3, lines 30-32). This range overlaps with the claimed range in the instant application of a thickness for the inner portion to occupy less than 75% of the floating gate thickness. (See MPEP 2144.05).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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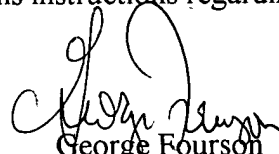
however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Closing

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956. **See MPEP 203.08.**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Barbara Elizabeth Abbott whose telephone number is (703) 306-5866. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax number for this group is (703)308-7722(and 7724 and 7382). MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.


George Fourson
Primary Examiner
Art Unit 2823


B.E. Abbott
October 10, 2000